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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/898,431	GRANIK ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 20-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 20-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14,20-29 were examined.

Section I: Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 10/25/2007 has been entered.

Section II: Non-Final Rejection

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-14, and 20-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al., (US Patent 6,544,699; hereafter Kim). Kim teaches a method for improving the accuracy of model-based optical proximity correction (OPC) (abstract).

Claim 1. A method of compensating mask/reticle data ("mask error effect can be

checked, column 5, lines 58-60) for lithographic process distortions ("empirical data...process distortions", column 2, lines 30-35), comprising the acts of: reading a set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) that defines at least one feature to be created lithographically (column 2, lines 56-63); performing an etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) of etch effects (column 2, lines 23-25) that would occur if a wafer (columns 4-5, lines 66-67 and 1-3, respectively) is exposed ("selected exposure", column 4, lines 44-50) using a mask/reticle corresponding to the set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) and etched with an etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50); using results of the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) to produce a revised set (if an improvement is conducted then the event is revised, "...method of improving the accuracy of... OPC", column 4, lines 20-26)of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) that are compensated for the etch effects (column 2, lines 23-25)and performing optical process correction (OPC) (column 4, lines 20-25)to produce a set of OPC-corrected mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) that compensate for optical/resist process distortions using the etch-compensated set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) as target layer (disclosure defines the target layer as the original layer to which the design layout is the original layout, "design layout"

column 2, lines 15-25)for the OPC.

Claim 2. The method of Claim 1, comprising an additional act of exporting the OPC-corrected set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) to a mask/reticle writer to manufacture a corresponding mask/reticle.

Claim 3. The method of Claim 1, in which the act of performing the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) includes accessing a set of predetermined rules ("optical rules checker", column 1, line 59) for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 4: The method of Claim 1, in which the act of performing the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) includes accessing a table of predetermined values for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 5. A method of compensating mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)for lithographic process distortions ("empirical data...process distortions", column 2, lines 30-35), comprising the acts of: reading

an initial set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)that defines at least one feature to be created lithographically (column 2, lines 56-63); performing an etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62)of etch effects (column 2, lines 23-25)that would occur if a wafer (columns 4-5, lines 66-67 and 1-3, respectively) is exposed ("selected exposure", column 4, lines 44-50) using a mask/reticle corresponding to the initial set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)and etched with an etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50); calculating etch biases from results of the etch simulation; and applying the calculated etch biases that are calculate from the initial set of mask/recticle data within a model-based optical process correction (OPC) (column 4, lines 20-25)loop that adjusts the mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)for optical/resist process distortions.

Claim 6 The method of Claim 5, in which the act of performing the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) includes accessing a set of predetermined rules ("optical rules checker", column 1, line 59) for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 7. The method of Claim 5, in which the act of performing the etch simulation ("lithographic imaging and semiconductor process simulation..."

column 2, lines 59-62) includes accessing a table of predetermined values for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 8: A computer-readable media having a sequence of programmed instructions stored thereon that when executed by a computer causes the computer to perform the acts of: reading a set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) that defines at least one feature to be created lithographically (column 2, lines 56-63); performing an etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) of etch effects (column 2, lines 23-25) that would occur if a wafer (columns 4-5, lines 66-67 and 1-3, respectively) is exposed ("selected exposure", column 4, lines 44-50) using a mask/reticle corresponding to the set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)and etched with an etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50) using the results of the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62)to produce a revised set (if an improvement is conducted then the event is revised, "...method of improving the accuracy of... OPC", column 4, lines 20-26)of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)that are compensated for the etch effects (column 2, lines 23-25)performing optical process correction (OPC) (column 4, lines 20-25)to produce a set of OPC-corrected mask/recticle data compensate for optical/resist process distortions

using the etch-compensate for optical/resist process distortions using the etch-compensated set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)as an input a target layer (disclosure defines the target layer as the original layer to which the design layout is the original layout, "design layout" column 2, lines 15-25)for the OPC.

Claim 9. The computer-readable media of Claim 8, wherein the sequence of programmed instructions causes the computer to export OPC- corrected mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) to a mask/reticle writer to manufacture a corresponding mask/reticle.

Claim 10. The computer readable media of Claim 8, in which the act of performing the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) includes accessing a set of predetermined rules ("optical rules checker", column 1, line 59) for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 11. The computer readable media of Claim 8, in which the act of performing the etch simulation includes accessing a table of predetermined values for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 12. A computer readable media having a sequence of programmed instructions stored thereon that when executed by a computer causes the computer to perform the acts of: reading an initial set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)that defines at least one feature to be created lithographically (column 2, lines 56-63); performing an etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62)of etch effects (column 2, lines 23-25)that would occur if a wafer (columns 4-5, lines 66-67 and 1-3, respectively) is exposed ("selected exposure", column 4, lines 44-50) with a mask/reticle corresponding to the set of initial mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)and etched with an etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50); calculating etch biases from results of the etch simulation; and applying the etch biases that are calculated from the initial set of mask/recticle data in a model-based optical process correction (OPC) (column 4, lines 20-25)loop that adjusts the mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)for optical/resist process distortions.

Claim 13 The computer readable media of Claim 12, in which the act of performing the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) includes accessing a set of predetermined rules ("optical rules checker", column 1, line 59) for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with

its dimensions, column 4, lines 44-50).

Claim14 The computer readable media of Claim 12, in which the act of performing the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) includes accessing a table of predetermined values for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 20. A device that is formed on a wafer (columns 4-5, lines 66-67 and 1-3, respectively) created by the acts of: reading a set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)that defines at least one feature to be created lithographically (column 2, lines 56-63); performing an etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) of etch effects (column 2, lines 23-25) that would occur if a wafer (columns 4-5, lines 66-67 and 1-3, respectively) is exposed ("selected exposure", column 4, lines 44-50) using a mask/reticle corresponding to the set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)and etched with an etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50); using results of the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62)to produce an a revised set (if an improvement is conducted then the event is revised, "...method of improving the accuracy of... OPC", column 4, lines 20-26)of

mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) that are compensated for the etch effects (column 2, lines 23-25) performing optical process correction (OPC) (column 4, lines 20-25) to produce OPC-corrected mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)that are compensated for optical/resist process distortions using revised set (if an improvement is conducted then the event is revised, "...method of improving the accuracy of... OPC", column 4, lines 20-26)of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) as target layer (disclosure defines the target layer as the original layer to which the design layout is the original layout, "design layout" column 2, lines 15-25)for the OPC; exporting the OPC-corrected set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) to a mask/reticle writer to manufacture a corresponding mask/reticle; and using the mask/reticle to create the device on the wafer (columns 4-5, lines 66-67 and 1-3, respectively).

Claim 21 The device of Claim 20, in which the act of performing the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) includes accessing a set of predetermined rules ("optical rules checker", column 1, line 59) for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 22. The device of Claim 20, in which the act of performing the etch

simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) includes accessing a table of predetermined values for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 23. A device that is formed on a wafer (columns 4-5, lines 66-67 and 1-3, respectively) created by the acts of: reading an initial set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)that defines at least one feature to be created lithographically (column 2, lines 56-63); performing an etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62) of etch effects that would occur if a wafer (columns 4-5, lines 66-67 and 1-3, respectively) is exposed ("selected exposure", column 4, lines 44-50) using a mask/reticle corresponding to the initial set of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)and etched with an etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50); calculating etch biases from results of the etch simulation; applying the etch biases that are calculated from the initial set of mask/recticle data within a model-based optical process correction (OPC) (column 4, lines 20-25)loop that adjusts the mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)for optical/resist process distortions; exporting the adjusted mask/reticle data ("mask error effect can be checked, column 5, lines 58-60)to a mask/reticle writer to create a corresponding mask/reticle; and using the mask/reticle to create the device on a wafer (columns 4-5, lines 66-67 and 1-3, respectively).

Claim 24. The device of Claim 23, in which the act of performing a simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62)includes accessing a set of predetermined rules ("optical rules checker", column 1, line 59) for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 25. The device of Claim 23, in which the act of performing the etch simulation includes accessing a table of predetermined values for the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50).

Claim 26. The method of Claim 1, wherein the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62)determines an increase in size (design choice) of a feature that would be created on a wafer (columns 4-5, lines 66-67 and 1-3, respectively) compared with a target feature size as a result of the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50) and a corresponding feature in the revised set (if an improvement is conducted then the event is revised, "...method of improving the accuracy of... OPC", column 4, lines 20-26) of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) is biased with a corresponding decrease in size (design choice).

Claim 27. The method of Claim 1, wherein the etch simulation ("lithographic imaging and semiconductor process simulation..." column 2, lines 59-62)determines a decrease in size (design choice) of a feature that would be created on a wafer (columns 4-5, lines 66-67 and 1-3, respectively) compared with a target feature size as a result of the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50) and a corresponding feature in the revised set (if an improvement is conducted then the event is revised, "...method of improving the accuracy of... OPC", column 4, lines 20-26) of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) is biased with a corresponding increase in size (design choice).

Claim 28. The computer readable media of Claim 8, wherein the instructions further cause the computer to determine an increase in size (design choice) of a feature that would be created on a wafer (columns 4-5, lines 66-67 and 1-3, respectively) compared with a target feature size as a result of the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50) and a corresponding feature in the revised set (if an improvement is conducted then the event is revised, "...method of improving the accuracy of... OPC", column 4, lines 20-26) of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) is biased with a corresponding decrease in size (design

choice).

Claim 29. The computer readable media of Claim 8, wherein the instructions further cause the computer to determine a decrease in size (design choice) of a feature that would be created on a wafer (columns 4-5, lines 66-67 and 1-3, respectively) compared with a target feature size as a result of the etch process (fabrication part of the etching process column 4, lines 3-6 dealing with its dimensions, column 4, lines 44-50) and a corresponding feature in the revised set (if an improvement is conducted then the event is revised, "...method of improving the accuracy of... OPC", column 4, lines 20-26) of mask/reticle data ("mask error effect can be checked, column 5, lines 58-60) is biased with a corresponding increase in size (design choice).

Section III: Response to Arguments

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5. Applicants are thanked for addressing these issues. Rejection is withdrawn.

102(e)

6. Applicants are thanked for addressing these issues; however, applicants' response is non-persuasive in view of the prior art. Arguments regarding the limitation "compensating mask/recticle..." is now moot by applicants' amendment (applicants' response, pg. 7 of 9, 3rd paragraph, line 7). The target layer is defined in applicants'

disclosure as the original layer (specification, paragraph [0005]) thus is inherent step of performing an OPC process; same logic applies to "reading the initial mask/reticle data" since a computer-based simulation event incorporates reading said data. Rejection, as set forth above, stands.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. David Vincent 571-272-3080. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

11/13/07

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